An 18-71 GHz Multi-band and High Gain GaAs MMIC Medium Power Amplifier for Millimeter-wave Applications

Pei-Si Wu, Tian-Wei Huang, *Senior Member, IEEE,* and Huei Wang, *Senior Member, IEEE*

Dept. of Electrical Engineering and Graduate Institute of Communication Engineering,
National Taiwan University, Taipei, Taiwan 106, R.O.C.

Abstract — **This paper presents the design and measurement results of a broadband high gain MMIC medium power amplifier. The proposed 18-71 GHz multi-band amplifier provides a single chip solution for all 28 GHz, 38 GHz, and 60 GHz millimeter-wave applications with a chip size of 2.5 mm x 1 mm. The high gain performance of more than 20 dB from 41-63 GHz has been attained. It provides at least 16 dBm of maximum output power from 19-57 GHz. This amplifier consists of one distributed stage for broadband design and cascaded single-ended stages for medium power output. This chip demonstrates the highest frequency application using this combined topology compared with all previously published results. The circuit was fabricated with a 0.15-μm gate-length GaAs-based HEMT MMIC technology.**

I. Introduction

In recent years, there are increasing demands of low-cost MMICs for microwave and millimeter-wave communication systems, such as LMDS (Local Multipoint Distribution Service) at 28 GHz, wireless communication systems at 38 GHz, and future broadband systems at 60 GHz. Therefore, it is desirable to design an amplifier that covers several frequency ranges at a low cost. In this paper, the proposed 18-71 GHz broadband amplifier provides a single chip solution for all above-mentioned millimeter-wave frequency bands with a chip size of 2.5 mm x 1 mm. The high gain performance of more than 20 dB from 41-63 GHz has been attained.

Several techniques have been utilized to realize a broadband MMIC amplifier. Feedback technique, which is mostly used below 50 GHz, serves either as resistive feedback [1]-[2] or feedback in core gain cell [3]. For 50 GHz and above, cascaded single stage designs can also achieve wideband performance [4]-[6]. As for broadband applications, distributed amplifiers represent a typical circuit solution to cover a wide frequency range [7]-[12]. Nevertheless, in the HEMT or HBT MMIC process, especially due to the C_{gs} or C_{be} of the devices, limits gain-bandwidth product of a distributed amplifier. Using large-size devices, distributed amplifiers can also be used for medium power designs; however, due to the power dissipation in drain-line termination, the power-added-efficiency (PAE) will be degraded significantly. To overcome these limitations, a distributed input stage for wideband and cascaded single-ended stages for high gain and large power may be used [13]-[15]; however, this approach has not been implemented over 45 GHz. In this paper, the medium power amplifier has a measured average gain of 20 dB between 18 to 71 GHz, and maximum output power over 16 dBm between 19 to 57 GHz.

II. HEMT Device Characteristics and MMIC Technology

The circuit is fabricated using 0.15-μm GaAs HEMT MMIC process provided by WIN Semiconductors. The unit current gain frequency (f_T) of the device is about 85 GHz, and the maximum oscillation frequency is over 200 GHz. Typical breakdown voltage is 10 V and the peak of transconductance is 495 mS/mm. Other passive components such as thin-film resistors, MIM capacitors, spiral inductors, and air-bridges are available. The 6" wafer is thinned down to 4-mil for the gold plating of the backside, and slot via holes are used for dc grounding.

III. Circuit Design

The amplifier consists of three stages of amplification. The first stage utilizes a distributed topology with two 2-finger 50-μm HEMT devices. The second and last stage utilizes 2-finger 100-μm and 4-finger 200-μm device, respectively.

The first stage utilizes two distributed cells to provide broadband gain for this design. The second and third stage is matched for large output power and wide bandwidth. The matching networks are realized with the inductive T-transformer using high and low impedance microstrip lines. The output matching network of the last stage utilizes LC distributed matching for wide output power bandwidth. The radial stubs provide small shunt capacitors for high frequencies. DC bias network utilizes 0.5 pF bypass to ground and shunt RC for low band decoupling. The passive circuits include the transmission

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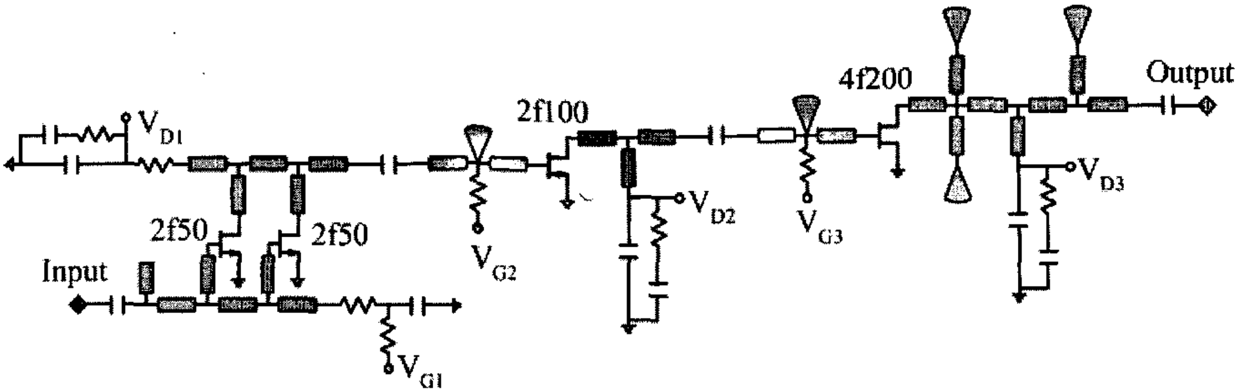

Fig. 1. Schematic of the medium power amplifier.

line discontinuities, radial stubs and capacitors, were simulated by a full-wave EM simulator (Sonnet software). The whole circuit of the amplifier was simulated by the circuit simulator (HP/EEsof Libra). Fig. 1 shows the schematic of the complete three-stage amplifier, and the chip photo is shown in Fig. 2. The chip size is 2.5 mm x 1 mm.

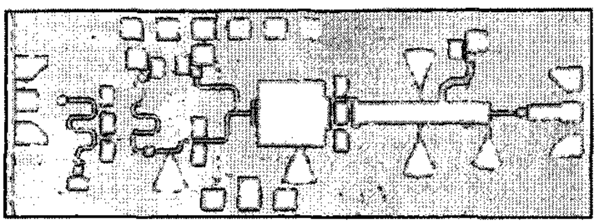

Fig. 2. Chip photo of the three-stage amplifier (Chip size 2.5 x 1 mm^2).

IV. Circuit Measurements and Discussion

The circuit was tested via on-wafer probing. Because of the restriction of the measurement system, this broadband performance was measured using two set-ups: we utilized HP8510C coaxial-type measurement system to measure 50 GHz and below, and the performance from 50 GHz to 75 GHz was measured in a V-band WR15 waveguide measurement system. The measured small-signal gain and return losses are shown in Fig. 3. The average small-signal gain is 20 dB from 18 GHz to 71 GHz. The bias condition for small-signal data was V_{D1} = 2 V, $V_{D2} = V_{D3}$ = 2.5 V, $V_{G1} = V_{G2} = V_{G3}$ = -0.3 V, and a total drain current of 130 mA. The total power consumption was 306 mW. The second and third single-ended stage of this amplifier is a band pass design; therefore it has no gain at low frequency.

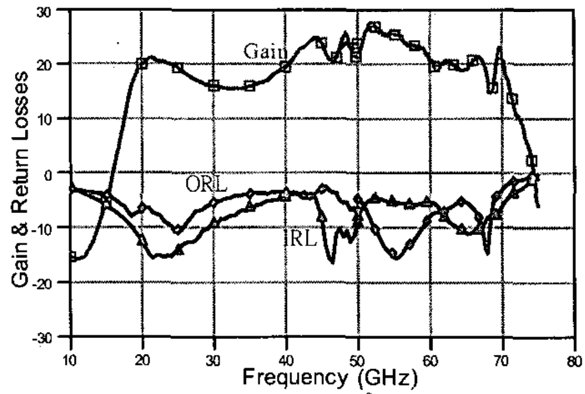

Fig. 3. Measured small-signal gain and return losses of the amplifier (V_{D1} = 2 V, $V_{D2} = V_{D3}$ = 2.5 V, $V_{G1} = V_{G2} = V_{G3}$ = -0.3 V).

Power performance for this amplifier was also measured. We utilized HP83650B signal generator and a power amplifier for large RF input power up to 50 GHz. From 50 GHz to 70 GHz, we utilized V-band HP85105A millimeter wave test set as the RF source. A variable attenuator was placed after the RF source, to lower its input power level. Fig. 4 shows output power versus input power of the amplifier at 20 GHz, 30 GHz, 40 GHz, 51 GHz, 60 GHz, and 70 GHz. The bias condition of Fig. 4 is the same as small-signal data. The saturation power (P_{sat}) versus frequency results are shown in Fig 5. The saturation power of the amplifier is at least 16 dBm from 19 to 57 GHz. The bias point of Fig. 5 power data was V_{D1} = 2.5 V, $V_{D2} = V_{D3}$ = 5 V, $V_{G1} = V_{G2} = V_{G3}$ = -0.23 V, and a total bias current was 138 mA.

Table I summarizes the reported performances of high gain and wideband amplifiers in high frequency ranges. It is observed that cascaded single-ended designs can achieve high gain, broadband, and large power, but cannot achieve all of them in the same time. On the other hand, gain-bandwidth product of a distributed amplifier is limited by the process. In order to achieve high gain, broadband, and large power simultaneously, we adopt one distributed stage and two single-ended stages. This approach has not implemented over 45 GHz, while we extend it up to 71 GHz.

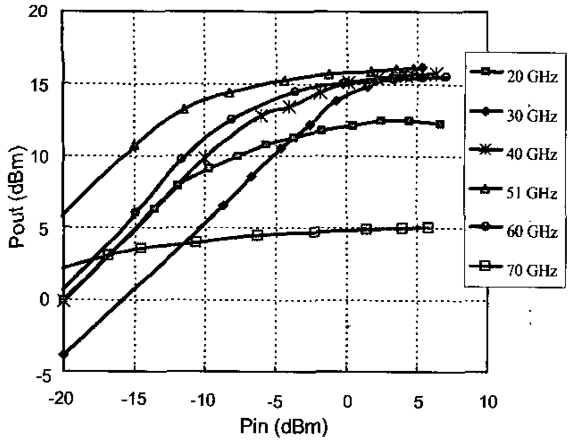

Fig 4. Output power versus input power for the medium power amplifier (V_{D1} = 2 V, V_{D2} = V_{D3} = 2.5 V, V_{G1} = V_{G2} = V_{G3} = -0.3 V).

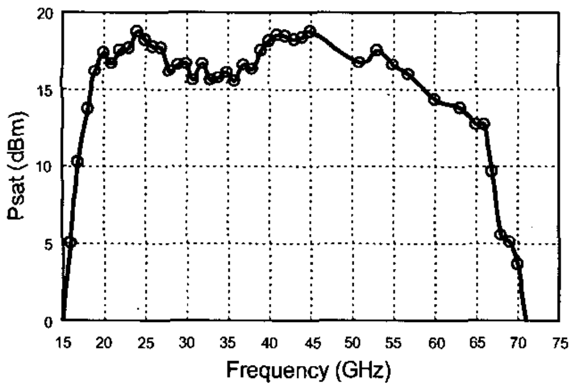

Fig. 5. Saturation power versus frequency for the medium power amplifier (V_{D1} = 2.5 V, V_{D2} = V_{D3} = 5 V, V_{G1} = V_{G2} = V_{G3} = -0.23 V).

V. SUMMARY

An 18-71 GHz high gain GaAs MMIC medium power amplifier has been designed, fabricated, and measured. It provides a single chip solution for all 28 GHz, 38 GHz, and 60 GHz millimeter-wave applications. The high gain performance of more than 20 dB from 41-63 GHz has been achieved. This amplifier can provide at least 16 dBm of maximum output power from 19 GHz to 57 GHz. The amplifier consists of one distributed input stage for wideband, two single-ended stages for high gain and large output power. This type of design can be improved for flat gain and large output power such as 20 dBm or above in the future.

ACKNOWLEDGEMENT

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Cascaded single-ended amplifiers					
Ref.	Frequency (GHz)	Gain (dB)	Process	P_{sat} (dBm)	Chip Size (mm^2)
[4]	48-60	22	0.15 μm GaAs HJFET	22	3.37 x 1.07
[5]	65-145	> 9	0.1 μm InP HEMT	17	1.2 x 1.4
[6]	75-110	> 10	0.1 μm GaAs HEMT	15	2.3 x 1.2
High gain distributed amplifiers					
[7]	0.1-65	15	0.15 μm GaAs MHEMT	N/A	1.36 x 1.17
[8]	0.001-54	15	0.15 μm GaAs HEMT	23	2.7 x 2.25
[9]	DC-92	13	0.1 μm InP HEMT	N/A	2.5 x 1.22
[10]	0.1-70	17	0.1 μm InP HEMT	11	N/A
[11]	0-74	13	InP HBT	10	1.7 x 0.45
[12]	0-93	23	InP D-HBT	N/A	1.65 x 0.755
Combined single-ended and distributed amplifiers					
[13]	17-40	21	GaAs HEMT	21	1.72 x 0.88
[14]	18-40	12.5	GaAs HEMT	14	1.44 x 1.064
[15]	20-44	22	GaAs HEMT	21	1.72 x 0.76
This work	18-71 41-63	>15(average 20) > 20	0.15 μm GaAs HEMT	16	2.5 x 1

Table I. Reported performances of high gain and broadband amplifiers in high frequency ranges.